ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Linear Classification Function Emulated by Pectin-Based Polysaccharide-Gated Multiterminal Neuron Transistors

Jianmiao Guo, Yanghui Liu, Feichi Zhou, Fangzhou Li, Yingtao Li, and Feng Huang**

Neuromorphic computing, which merges learning and memory functions, is a new computing paradigm surpassing traditional von Neumann architecture. Apart from the plasticity of artificial synapses, the simulation of neurons' multi-input signal integration is also of great significance to realize efficient neuromorphic computing. Since the structure of transistors and neurons is strikingly similar, capacitively coupled multi-terminal pectin-gated oxide electric double layer transistors are proposed here as artificial neurons for classification. In this work, the free logic switching of "AND" and "OR" is realized in the device with triple in-plane gates. More importantly, the linear classification function on a single neuron transistor is demonstrated experimentally for the first time. All the results obtained in this work indicate that the prepared artificial neuron can improve the efficiency of artificial neural networks and thus will play an important role in neuromorphic computing.

1. Introduction

Unlike traditional von Neumann architecture of which the computation module is kept separate from memory, human brain has the ability to complete learning and memory orders simultaneously and in parallel to ensure effective processing of information with low energy consumption.[1–4] For the internal mechanism, there are $\approx 10^{11}$ neurons existing in our brain and each of them can be connected to thousands of others through dendrites.[5] This interconnection creates an intricate neural network, which forms the physiological basis of human perception, thought, and behavior.[6] Thousands of input signals which reach different dendrites at the same time can be received by a single neuron, and all these signals will be integrated by soma to generate an action potential which is then transmitted to other neurons via synapses. Due to this integration effect, the capacity of information processing and the efficiency of the biological nervous system are greatly enhanced. Therefore, in order to realize both energy-saving and effective artificial neural networks and systems, it is necessary to develop neuromorphic devices with information integration ability.[7]

In the field of machine learning, the mechanism of statistical classification is to identify and classify one object on the basis of its features.[8] A linear classifier can achieve the aim of classification just through a specific "hyperplane", which makes its advantages in simplicity and high effect speed obvious. The essence of the linear classifier is a single-layer neural network, which is the basis of constructing multi-layer neural networks and implementing complex functions such as image recognition and speech recognition. In general situations, classification functions mainly depend on standard von Neumann machines and complex algorithms, but the parallel computing capability of this method is constrained. Therefore, if it is a single neuromorphic device that can be used as a linear classifier, the performance of the neuromorphic computing system would be greatly improved then.

With the rapid development of neuromorphic engineering, many functions including logic operations,[9–16] sound location functionality,[17] spatiotemporal information processing,[18–22] artificial efferent nerves,[23,24] and the simulation of multiple transmissions of various neurotransmitters in the human brain[25,26] have been implemented by researchers. Compared with two-terminal artificial synaptic devices, the configuration of transistors is more similar to that of neurons, which thus brings great potential to transistors' being used to imitate various functions of neurons.[27–37] In particular, the electric double layer (EDL) transistor, which can operate with extremely low power consumption due to its huge EDL capacitance,[38] shows its superiority. Besides, the extremely powerful electrostatic coupling capability allows us to design multi-gate transistors to realize the dendritic function of neurons, which is of great application significance in the field of neuromorphic computing.[18,39,40]

In this work, we constructed a neuron transistor that can integrate multiple input signals and thus can be used as an artificial neuron. The pectin polysaccharide-gated oxide EDL transistor with multiple in-plane gates were prepared by a simple solution method. By being connected with a resistor, the pectin neuron transistor can be used as a resistor-loaded inverter, and

J. Guo, Prof. Y. Liu, F. Li, Y. Li, Prof. F. Huang
State Key Laboratory of Optoelectronic Materials and Technologies
School of Materials
Sun Yat-sen University
Guangzhou 510275, P. R. China
E-mail: liuyanghui@mail.sysu.edu.cn; huangfeng@mail.sysu.edu.cn
Prof. F. Zhou
School of Microelectronics
Southern University of Science and Technology
Shenzhen 518055, P. R. China

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202102015.

DOI: 10.1002/adfm.202102015

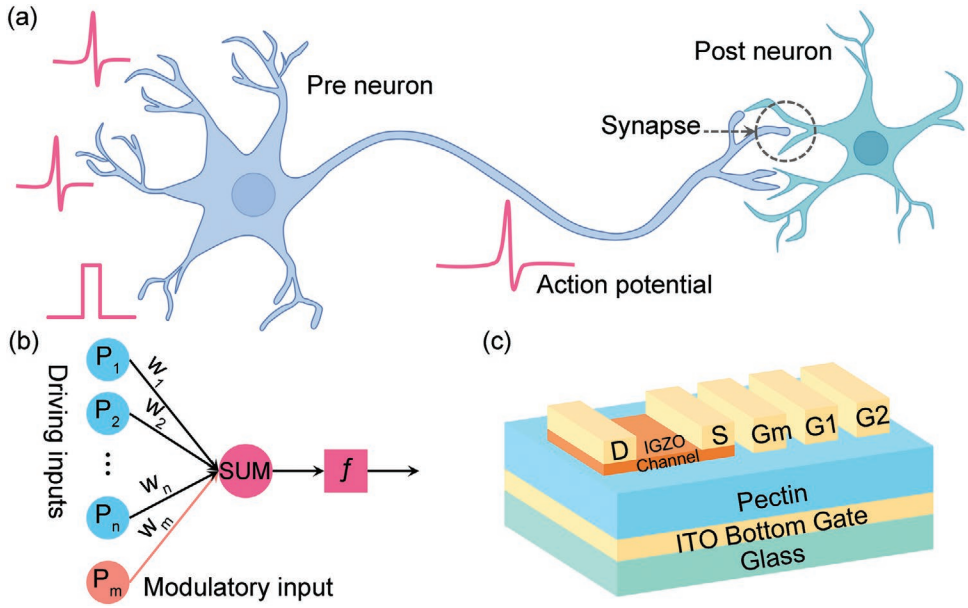

Figure 1. Structure diagrams of biological neuron system and the multi-terminal pectin-gated neuron transistor. a) Representation of a biological neuron from pre-neuron to post-neuron. b) One of the most representative mathematic neuron models. The w_i (i = 1, 2...*n* and *m*) represents the synaptic weight of each input. c) Schematic structure of a multi-terminal pectin-gated neuron transistor. The multiple in-plane gates are regarded as presynaptic input terminals and the channel conductance is regarded as output.

the multi-gate transistor can be used to demonstrate logic operations. More specifically, for the first time, a linear classification function is implemented on a single pectin neuron transistor. This neuromorphic device with multi-input integration can greatly enhance the information processing efficiency of artificial neurons and is of great significance to the realization of artificial neuromorphic systems. Besides, this single-layer neural network has the potential to be used to build multi-layer neural networks to realize more complex neural functions, such as visual image processing and understanding, pattern recognition, etc.

2. Results and Discussion

In the biological nervous system, a typical neuron consists of three function components including soma, dendrite, and single axon, as shown in **Figure 1**a. A neuron is linked to other neurons via thousands of dendrites and synapses and affected by the input signals received by dendrites, the soma generates an action potential which is then transmitted to other neurons by an axon through synapses.[41,42] Figure 1b shows a neuron mathematical model with dendritic integration function, which describes the process of multiple parallel inputs' being summed up and output by a node of summing junction. Here, we propose a multi-gate pectin-gated oxide EDL transistor for emulating simple neuron functions, whose structure schematic illustrated on indium tin oxide (ITO) glass is shown in Figure 1c. Here is a general and simple explanation of this mechanism, that is, the in-plane gates are regarded as the dendrites to receive signal inputs, and the channel conductance is considered as the output, where the carriers will be induced by the enormous EDL capacitance to accumulate through the strong proton/electron coupling ability. Such ability ensures that the EDL transistor owns the potential to simulate neuron functions.

Material quality is the key factor in device performance, so we first performed a series of characterizations on the pectin films prepared by the solution process, as shown in **Figure 2**. Figure 2a shows the atomic force microscopy (AFM) surface scanning morphology of the pectin film, where the root mean square roughness of 6.9 nm proves the flatness of this film surface. Figure 2b is the cross-sectional scanning electron microscopy (SEM) morphology of the pectin film, from which a uniform 0.9 µm-thick film without any holes or cracks is observed and thus the surface smoothness is confirmed again. Figure 2c is the Fourier Transform Infrared (FTIR) spectrum of the pectin film. In the illustration, the valley point found at 3500 cm^{-1} originates from the stretching vibration of –OH which helps with protons migration in the gate dielectric. Besides, the volley points at 2950 and 1750 cm^{-1} correspond to C–H tensile vibration and C=O tensile vibration, respectively, and the volley points at 1640 and 1400 cm^{-1} match with the COO- tension vibration. The pattern in the fingerprint region is similar to that found in previous work,[43] which confirms that the functional groups of pectin will not change before and after film formation. What's more, as the gate dielectric of EDL transistors, pectin film should have a low leakage current within the working voltage range of the device. To obtain the leakage current of this pectin film, we used a sandwich structure of ITO/pectin/ITO to conduct this test with the results shown in Figure 2d, from which it can be seen that the leakage current density of the device is less than 0.8 µA cm^{-2} in the range of –20 to 20 kV cm^{-1}, which ensures that the device will not be broken down in the field-effect mode.

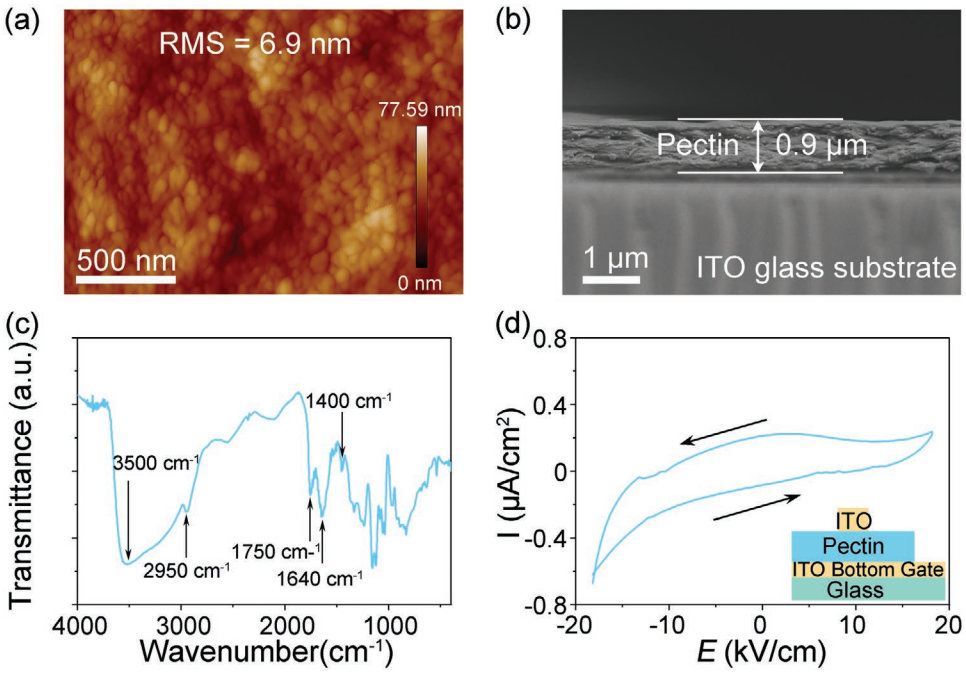

Figure 2. Characterizations of the solution-processed pectin film. a) AFM image of the pectin film on the ITO glass substrate. The root mean square roughness is 6.9 nm, showing a smooth surface. b) Cross-sectional SEM image of the pectin film on the Si substrate. The thickness is estimated to be 0.9 μm, which is noted in the figure. c) FTIR spectrum of the pectin film. d) Leakage current density curves of the pectin film. The inset shows the ITO/pectin/ITO sandwich structure used in the test.

Figure 3a shows the output characteristics of a pectin-gated EDL transistor (whose structure schematic is shown in the inset) operating in bottom-gate mode with V_{GS} swept from 0 to 1.4 V in 0.2 V steps. In the low-V_{DS} region, I_{DS} increases linearly

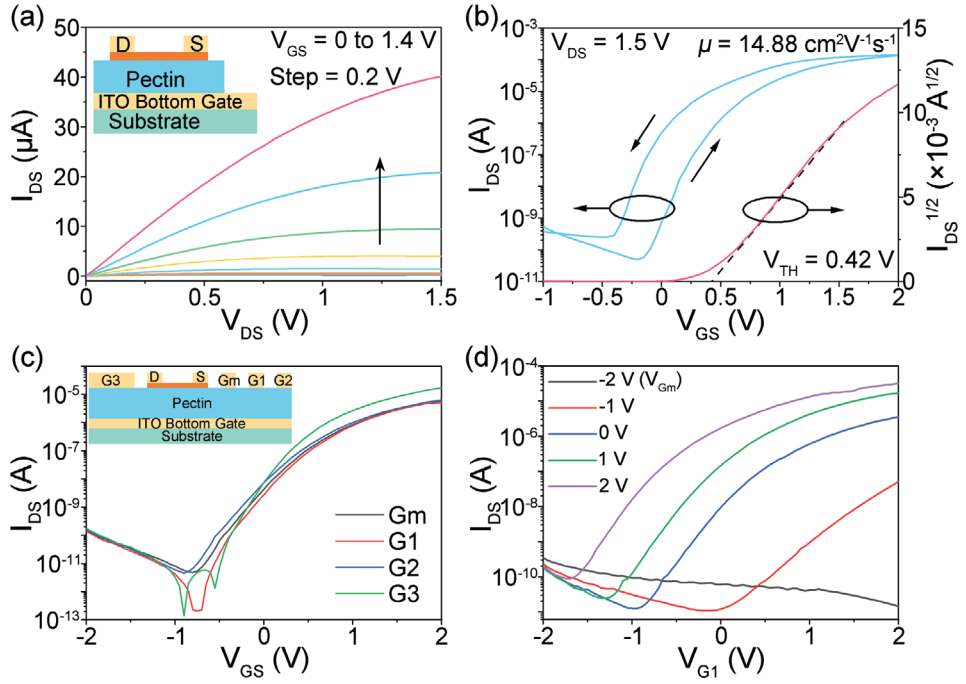

Figure 3. Basic electrical properties of the pectin-gated EDL transistor. a) The output characteristics of the pectin-gated EDL transistor and the schematic (inset) of the bottom-gate transistor. b) The transfer characteristics of the pectin-gated EDL transistor with a bottom gate measured at a fixed V_{DS} of 1.5 V. c) The transfer characteristics of the pectin-gated EDL transistor with different in-plane gates and the schematic (inset) of the transistor with in-plane gates. Gate electrode area: Gm = G1 = G2 = 1/3G3. d) Transfer curves of the pectin-gated EDL transistor measured with a sweep voltage applied to G1 and modulatory voltages applied to Gm.

with V_{DS}, indicating that there is good ohmic contact between the indium gallium zinc oxide (IGZO) channel layer and the ITO electrode. When V_{DS} continues to increase, I_{DS} tends to be saturated. Figure 3b shows the transfer characteristics of the transistor in the saturation region (V_{DS} = 1.5 V). A large current ON/OFF ratio of ≈10^6 and a small subthreshold swing (SS) (≈110 mV decade^{-1}) are obtained from the curve. According to the $I_{DS}^{1/2}$–V_{GS} curve, the threshold voltage (V_{TH}) is estimated to be about 0.42 V, and the field-effect carrier mobility (μ) is calculated to be ≈14.88 cm^2 V^{-1} s^{-1}.[44] Transfer curves with different V_{DS} range from 0.1 to 0.5 V are shown in Figure S2, Supporting Information. The results above indicate that the proposed pectin-gated transistor is a typical n-channel enhancement-type field-effect transistor. The inset in Figure 3c shows a schematic diagram of the pectin-gated EDL transistor operating in in-plane gate mode. Due to the strong electrostatic coupling effect, the voltage applied to the in-plane gate could be coupled to the IGZO channel layer. Figure 3c illustrates the transfer curves obtained using four different in-plane gates, from which it can be seen that the gates Gm, G1, and G2 show similar modulate capabilities, but G3 with a larger area shows stronger modulate ability with the signs of a reduction of SS and a larger I_{DS} achieved when V_{GS} = 2 V. Figure 3d shows the transfer curves of the fabricated transistor with two in-plane gate inputs (Gm and G1). When V_{Gm} = −2 V, I_{DS} remains below 1 nA in the range of V_{G1} from −2 to 2 V. With the increase of V_{Gm}, I_{DS} also increases, which shows that there is an effective coordinated modulation effect existing in the in-plane gates of this transistor.

First, basic synaptic plasticities were emulated by pectin-gated transistor (Figure S3, Supporting Information). Then, to study the potential of this fabricated device's being applied to logic operations, we connected a 10 MΩ resistor with the drain of the pectin-gated EDL transistor to construct a resistor-loaded inverter, as shown in **Figure 4**a. Equivalent circuit diagram is shown in Figure S4, Supporting Information. Corresponding voltage output characteristic curves at different V_{DD} are shown in Figure 4b. When V_{IN} is at a low voltage (logic "0"), the transistor is in an "OFF" state, and thus the channel resistance is much greater than the value of external resistance, causing most of the voltage to fall on the transistor and then a high voltage (logic "1") is output. On the contrary, a high V_{IN} can turn on the transistor, which will make most of the voltage fall on the external resistor and output a low voltage (logic "0"). More detailed explanation can be found in Figure S5, Supporting Information. As shown in Figure 4c, the corresponding voltage gains ($-dV_{OUT}/dV_{IN}$) rise with the increase of V_{DD}. For example, a high voltage gain of ≈20 can be obtained at a V_{DD} of 3.0 V. Figure 4d–f shows the dynamic performance of this inverter with various input signals (sine wave, triangle wave, and the square wave of 1 Hz) that are filtered by the inverter and then output identical square waves finally. Figure S6, Supporting Information indicates that the inverter shows good noise filtering characteristics with 0.2 V random noise and is suitable for working under low frequency.

The pectin-gated EDL transistor with a multi-gate structure could be used as an artificial neuron. Based on the pectin neuron transistor, simple signal integration functions have been realized. **Figure 5**a shows the circuit layout for implementing the linear classifier function. In the schematic, Gm is used as the control terminal, and the input voltage signal is applied to G1 and G2. Equivalent circuit diagram of the proposed linear classifier based on a tri-gated pectin neuron transistor is shown in Figure S7, Supporting Information. Figure 5b shows the spike logic operation of this device. When a voltage of 1 V is applied to Gm, the "OR" logic can be realized; when a voltage of −1 V is applied to Gm, the neuron transistors will perform an "AND" logic. Therefore, the switch between "OR" and "AND" logic can be easily shifted by changing the voltage applied to the control gate. Based on the spike logic operation functions above, the artificial pectin neuron transistors can also be used for data classification. We define the input data of two input terminals as a 2D space, where the function of a linear classifier is to classify the data with a straight line. Here, we define that if $V_{OUT} > 0$, the input data are interpreted as

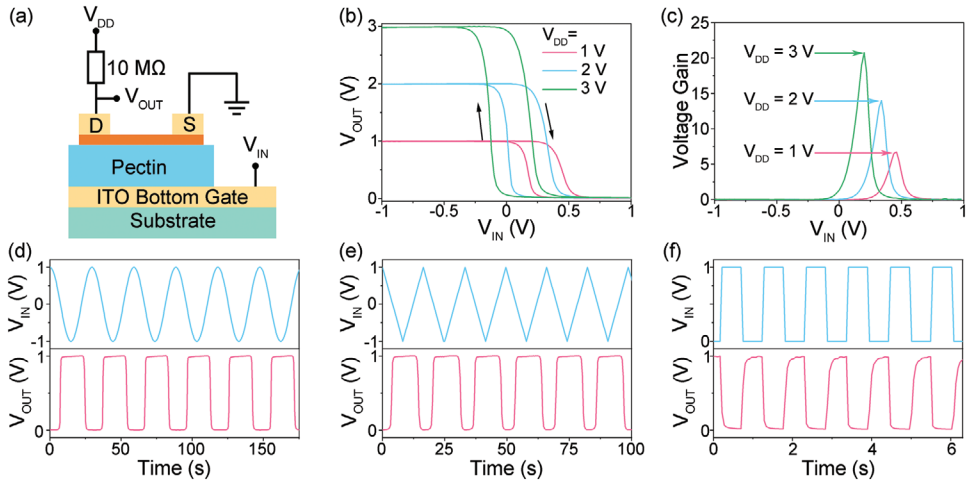

Figure 4. Logic modulation operations of the pectin-gated EDL transistor. a) Schematic diagram of resistor-loaded inverter working in bottom-gate mode with a 10 MΩ resistor. b) Voltage transfer characteristics of resistor-loaded inverter with different V_{DD} ranging from 1 to 3 V in 1 V steps. The V_{IN} sweep rate is 0.02 V·s^{-1}. c) Voltage gain ($-dV_{OUT}/dV_{IN}$) of the resistor-loaded inverter calculated from the forward scanning voltage transfer curves. The dynamic response of resistor-loaded inverter at V_{DD} = 1 V is shown here when V_{IN} signals are: d) sine, e) triangle, and f) pulse at 1 Hz.

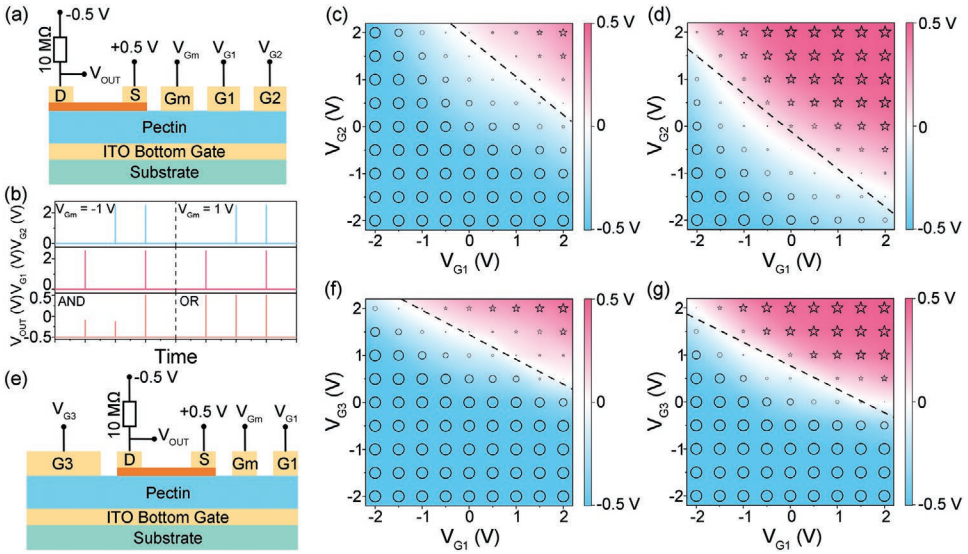

Figure 5. Data classifications function of the pectin-gated EDL transistor. a) Schematic diagram of the tri-gated device with a 10 MΩ resistor. Gm is used as a modulation terminal, while G1 and G2 are considered as input terminals. b) Input–output characteristics of the "OR" and "AND" logic operation, which can be shifted by the control signal V_{Gm}. Data classifications demonstrated by the pectin neuron transistor. The control gate Gm is biased at c) –1.0 and d) 1.0 V. The circle size and the stars represent the absolute value of data points. e) Schematic diagram of the tri-gated device, where G3 has replaced G2. Data classifications realized by the pectin-gated neuron transistor. The control gate Gm is biased at f) –1.0 and g) 1.0 V.

being in one class, otherwise, it is in another class. It can be clearly seen that when V_{Gm} = –1 V, the boundary of data classification is located in the upper right corner of data space with only a small part of the data being positive (Figure 5c). When a voltage of 1 V is applied to Gm, the classification boundary moves to the negative direction of the coordinate axis, as shown in Figure 5d. This means that the data classification rules can be shifted by changing the voltage applied to the control gate. Interestingly, the slope of the data classification boundary is about –1, which we guess is due to the same modulation ability of G1 and G2 gates. To verify this conjecture, we use a larger gate (G3) with a stronger modulation ability to replace G2 to be the input terminal (Figure 5e). As we predicted, the slope of the classification boundary is tilted toward the axis representing G3, as shown in Figure 5f,g. Stereogram of the linear classifier result can be found in Figure S8, Supporting Information. In summary, the classification boundary can be shifted horizontally by changing the voltage of the control gate, and the slope of the classification boundary can be altered by changing the area of the input gate electrode. Theoretically, the classification boundary with any slope can be located at any position in the 2D space. These findings clearly indicate that the in-plane gates of this device exhibit excellent potential for synergistic modulation, and also experimentally demonstrate the linear classification function for the first time by using a single pectin neuron transistor. Such devices can greatly simplify the design of artificial neural networks and neuromorphic systems. Based on the linear classification function, advertisement targeting, spam detection, medical diagnosis, and image classification could be further realized. Besides, multi-layer neural network constructed based on this single-layer neural network has the potential to achieve more complex neural functions efficiently.

The realization of logic operation function and linear classification function in pectin neuron transistors can be well explained by the movement of protons in the gate dielectric. **Figure 6**a shows the schematic diagram of the pectin neuron transistors working in in-plane gate mode. Figure 6b shows the graph of capacitance versus frequency obtained through four different structures. C0, C1, C2, and Cm show similar values (Figure S1, Supporting Information). Figure 6c is the frequency-dependent capacitance curve between the test frequencies from 1 to 10 Hz. It can be found that when the test frequency is 1 Hz, the capacitance between a single top electrode and bottom gate linearly depends on the area of the electrode (C3 ≈ 3C1). In addition, as the electrode area increases, the capacitance between two in-plane gates would also rise. When V_{Gm} = –1 V, the majority of protons will migrate to the pectin electrolyte/Gm interface with almost no protons staying at the channel/electrolyte interface. In this case, two higher inputs are needed to turn on the device ("AND" logic, Figure 6d). Conversely, when V_{Gm} = 1 V, part of the protons will migrate to the channel/electrolyte interface, and now only one high input is enough to reach the ON state ("OR" logic, Figure 6e). When V_{Gm} and V_{G2} are both fixed at 1 V, the number of protons induced by gate G1 with a smaller area (Figure 6f) and by gate G3 with a larger area (Figure 6g) at the gate/electrolyte interface is different, which is due to the difference in EDL capacitance (C03 > C01). In other words, the gate with a larger area is more capable of inducing protons at the gate dielectric/channel interface, which is consistent with the results of transfer curves previously measured by these gates. It is this different control ability that contributes to the slope change of the classification boundary in the linear classification function.

3. Conclusion

In summary, we use pectin polysaccharide as the electrolyte gate dielectric to fabricate neuron transistors with multiple in-plane

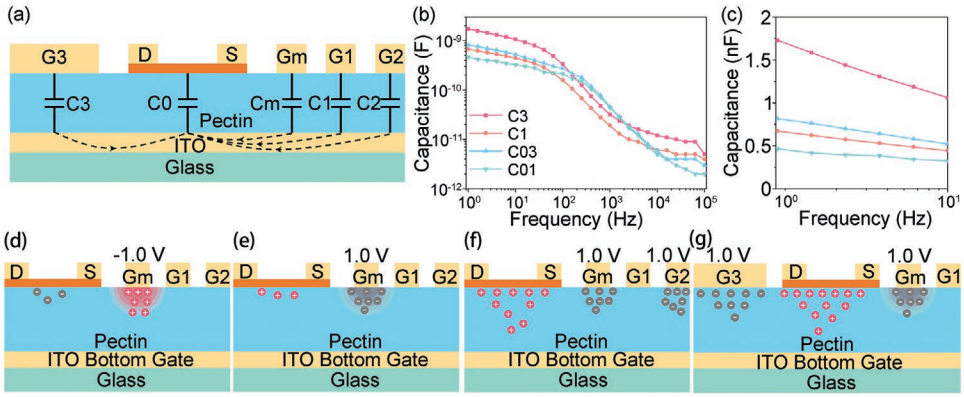

Figure 6. a) The schematic diagram of the pectin-gated EDL transistor working in in-plane gate mode. Gate electrode area: Gm = G1 = G2 = 1/3G3. b) Frequency-dependent capacitance of four different structures. C3, C1, C03, and C01 represent the capacitance obtained through G3/pectin/ITO, G1/pectin/ITO, drain/pectin/ITO/pectin/G3, and drain/pectin/ITO/pectin/G1 structures, respectively. C0, C1, C2, and Cm show similar values. c) Partially enlarged view of frequency-dependent capacitance. When the test frequency is 1 Hz, C3, C1, C03, and C01 are 1.73, 0.67, 0.82, and 0.47 nF, respectively. The schematics illustrate the proton distribution when d) $V_{Gm} = -1.0$ V and e) $V_{Gm} = 1.0$ V, respectively. And when V_{Gm} is fixed at 1 V, the schematic of the working mechanism is shown here when f) $V_{G2} = 1.0$ V and g) $V_{G3} = 1.0$ V, respectively.

gates on ITO glass substrates. On account of the extremely strong proton/electron coupling effect, the pectin-gated oxide EDL transistors exhibit excellent transistor performance. For the pectin-gated transistors working in a bottom-gate mode, inverter function and filtering function are realized; for the pectin-gated transistors working in in-plane gate mode, the free logic switching of "OR" and "AND" is realized, and the linear classification function of neurons is also achieved on a single device. All those functions are highly related to neuromorphic computing, so this type of transistors is of great significance to simplify the structure of neuromorphic computing systems and improving computing efficiency.

4. Experimental Section

Fabrication of Multi-Terminal Neuro-Transistors: The proposed pectin neuron transistors were fabricated on ITO glass substrates. First, pectin powder (Macklin) was dissolved in 10 mL deionized water and magnetically stirred at 60 °C for 2 h to obtain a 1.0 wt% homogeneous pectin solution. Then the pectin solution was drop-cast onto the ITO glass substrates and silicon substrates, and then dried at room temperature for 24 h to form solid pectin films with uniform thickness and smooth surface. Third, IGZO (molar ratio: In_2O_3:Ga_2O_3:ZnO = 1:1:1) was used as the growth source, and via RF magnetron sputtering, a patterned channel layer was deposited on the surface of the pectin film. The sputtering power, working pressure, Ar gas flow rate, and sputtering time were 100 W, 0.3 Pa, 15 sccm, and 30 min, respectively. Finally, the sputtering of the in-plane gates and source/drain electrodes was conducted using an ITO (In_2O_3:SnO_2 = 90%:10%) target with RF power, working pressure, Ar gas flow rate, and sputtering time were 50 W, 0.3 Pa, 15 sccm, and 2 min, respectively. The dimension of the electrodes was 1000 μm × 150 μm. The width and length of the channel layer were 1000 and 80 μm, respectively.

Characterization of Pectin Films: The surface roughness of the pectin film was measured by an atomic force microscope (CSPM 5500). The cross-sectional SEM morphology was characterized by a scanning electron microscope (Zeiss Auriga). The FTIR spectrum was analyzed by Shimadzu IRAffinity-1S. Frequency-dependent capacitance of the pectin film was performed by applying a 0.1 V sinusoidal signal with a HIOKI IM 3533-01 LCR METER.

Device Electrical Characterization: The electrical characteristics of the transistors were measured at room temperature with a relative humidity of 50% by Keithley 4200A SCS. Keithley 2636B source meter was also used to test the data classification function of neuron transistors.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by National Natural Science Foundation of China (61904208 and 91833301).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

artificial neurons, electric double layer transistors, linear classification, multi-terminal neuromorphic devices

Received: February 27, 2021
Revised: April 9, 2021
Published online: June 14, 2021

[1] H. Markram, *Nat. Rev. Neurosci.* **2006**, *7*, 153.
[2] D. Querlioz, O. Bichler, A. F. Vincent, C. Gamrat, *Proc. IEEE* **2015**, *103*, 1398.

[3] C. K. Machens, *Science* **2012**, *338*, 1156.
[4] J. Backus, *Commun. ACM* **1978**, *21*, 613.
[5] J. C. Magee, *Nat. Rev. Neurosci.* **2000**, *1*, 181.
[6] V. M. Ho, J. A. Lee, K. C. Martin, *Science* **2011**, *334*, 623.
[7] J. M. Cruz-Albrecht, M. W. Yung, N. Srinivasa, *IEEE Trans. Biomed. Circuits Syst.* **2012**, *6*, 246.
[8] G. Yuan, C. Ho, C. Lin, *Proc. IEEE* **2012**, *100*, 2584.
[9] Y. H. Liu, L. Q. Zhu, P. Feng, Y. Shi, Q. Wan, *Adv. Mater.* **2015**, *27*, 5599.
[10] F. Shao, P. Feng, C. Wan, X. Wan, Y. Yang, Y. Shi, Q. Wan, *Adv. Electron. Mater.* **2017**, *3*, 1600509.
[11] C. J. Wan, Y. H. Liu, P. Feng, W. Wang, L. Q. Zhu, Z. P. Liu, Y. Shi, Q. Wan, *Adv. Mater.* **2016**, *28*, 5878.
[12] Y. Gao, X. Wang, J. Luo, Z. Liu, Q. Wan, *IEEE Electron Device Lett.* **2019**, *40*, 1205.
[13] X. Yang, Z. Liu, J. Luo, C. Zhang, Y. He, Y. Shi, Q. Wan, *IEEE Electron Device Lett.* **2020**, *41*, 1360.
[14] Z. Liu, S. Nie, J. Luo, Y. Gao, X. Wang, Q. Wan, *Adv. Electron. Mater.* **2019**, *5*, 1900235.
[15] Y. He, Y. Zhu, C. Chen, R. Liu, S. Jiang, L. Zhu, Y. Shi, Q. Wan, *IEEE Trans. Electron Devices* **2020**, *67*, 5216.
[16] Y. H. Liu, L. Q. Zhu, Y. Shi, Q. Wan, *Appl. Phys. Lett.* **2014**, *104*, 133504.
[17] Y. He, S. Nie, R. Liu, S. Jiang, Y. Shi, Q. Wan, *Adv. Mater.* **2019**, *31*, 1900903.
[18] C. J. Wan, L. Q. Zhu, Y. H. Liu, P. Feng, Z. P. Liu, H. L. Cao, P. Xiao, Y. Shi, Q. Wan, *Adv. Mater.* **2016**, *28*, 3557.
[19] C. Zhang, S. Li, Y. He, C. Chen, S. Jiang, X. Yang, X. Wang, L. Pan, Q. Wan, *IEEE Electron Device Lett.* **2020**, *41*, 617.
[20] S. Nie, Y. He, R. Liu, Y. Shi, Q. Wan, *IEEE Electron Device Lett.* **2019**, *40*, 459.
[21] J. Guo, Y. Liu, Y. Li, F. Li, F. Huang, *ACS Appl. Mater. Interfaces* **2020**, *12*, 50061.
[22] J. Jiang, J. Guo, X. Wan, Y. Yang, H. Xie, D. Niu, J. Yang, J. He, Y. Gao, Q. Wan, *Small* **2017**, *13*, 1700933.
[23] H. Wei, R. Shi, L. Sun, H. Yu, J. Gong, C. Liu, Z. Xu, Y. Ni, J. Xu, W. Xu, *Nat. Commun.* **2021**, *12*, 1068.
[24] K. He, Y. Liu, M. Wang, G. Chen, Y. Jiang, J. Yu, C. Wan, D. Qi, M. Xiao, W. R. Leow, H. Yang, M. Antonietti, X. Chen, *Adv. Mater.* **2020**, *32*, 1905399.
[25] S. Zhang, K. Guo, L. Sun, Y. Ni, L. Liu, W. Xu, L. Yang, W. Xu, *Adv. Mater.* **2021**, *33*, 2007350.
[26] T. Chen, P. A. Bobbert, W. G. van der Wiel, *Small Sci.* **2021**, *1*, 2000014.
[27] E. Baek, N. R. Das, C. V. Cannistraci, T. Rim, G. S. C. Bermúdez, K. Nych, H. Cho, K. Kim, C.-K. Baek, D. Makarov, R. Tetzlaff, L. Chua, L. Baraban, G. Cuniberti, *Nat. Electron.* **2020**, *3*, 398.
[28] J. Hasler, H. Marr, *Front. Neurosci.* **2013**, *7*, 118.
[29] Z. Wang, M. Rao, J.-W. Han, J. Zhang, P. Lin, Y. Li, C. Li, W. Song, S. Asapu, R. Midya, Y. Zhuo, H. Jiang, J. H. Yoon, N. K. Upadhyay, S. Joshi, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, Q. Qiu, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Commun.* **2018**, *9*, 3208.
[30] V. K. Sangwan, H.-S. Lee, H. Bergeron, I. Balla, M. E. Beck, K.-S. Chen, M. C. Hersam, *Nature* **2018**, *554*, 500.
[31] X. Yang, J. Yu, J. Zhao, Y. Chen, G. Gao, Y. Wang, Q. Sun, Z. L. Wang, *Adv. Funct. Mater.* **2020**, *30*, 2002506.
[32] F. Zhou, Y. Chai, *Nat. Electron.* **2020**, *3*, 664.
[33] F. Zhou, Y. Liu, X. Shen, M. Wang, F. Yuan, Y. Chai, *Adv. Funct. Mater.* **2018**, *28*, 1800080.
[34] F. Zhou, Z. Zhou, J. Chen, T. H. Choy, J. Wang, N. Zhang, Z. Lin, S. Yu, J. Kang, H. S. P. Wong, Y. Chai, *Nat. Nanotechnol.* **2019**, *14*, 776.
[35] L. F. Abbott, W. G. Regehr, *Nature* **2004**, *431*, 796.
[36] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
[37] J. Q. Yang, R. p. Wang, Y. Ren, J. Y. Mao, Z. P. Wang, Y. Zhou, S. T. Han, *Adv. Mater.* **2020**, *32*, 2003610.
[38] L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi, Q. Wan, *Nat. Commun.* **2014**, *5*, 3158.
[39] X. Wan, Y. Yang, Y. L. He, P. Feng, W. J. Li, Q. Wan, *IEEE Electron Device Lett.* **2017**, *38*, 525.
[40] Y. He, S. Nie, R. Liu, S. Jiang, Y. Shi, Q. Wan, *IEEE Electron Device Lett.* **2019**, *40*, 818.
[41] H. Kalita, A. Krishnaprasad, N. Choudhary, S. Das, D. Dev, Y. Ding, L. Tetard, H.-S. Chung, Y. Jung, T. Roy, *Sci. Rep.* **2019**, *9*, 53.
[42] C. Wan, Y. He, S. Jiang, J. Li, Q. Wan, *ACS Appl. Electron. Mater.* **2020**, *2*, 389.
[43] R. Gnanasambandam, A. Proctor, *Food Chem.* **2000**, *68*, 327.
[44] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.